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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,827	WEIS ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *52-67* is/are pending in the application.

4a) Of the above claim(s) *52-60* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *61-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment and RCE filed September 20, 2006. Claims 1-51 were canceled. Claims 52-60 have been newly added.

Election/Restrictions

1. Newly submitted method claims 52-60 are directed to an invention for method claims that is distinct from the invention originally invention for product claims 61-67, Group I, originally presented and elected. New method claim 52-60, Group II, is directed to a process, in which, for example, forming a line mask over the semiconductor body after forming the plurality of trenches. Since applicant originally elected product claims for consideration, without traverse, and has received an action on the merits for the originally presented invention of subject matter of product claims, this invention of Group I, claims 61-67 has been constructively elected by original presentation and examination for prosecution on the merits.

Accordingly, Group II, new method Claims 52-60, drawing to a method of making a semiconductor memory device is withdrawn from consideration as being directed to a non-elected invention, without traverse as treated and originally elected. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

2. Claims 61-67 are rejected under 35 U.S.C. 102(e) as being anticipated by Mandelman et al (6,339,241).

Re claim 61, Mandelman teaches a memory cell device comprising: an array of memory cells arranged an array of rows and columns at the surface of a semiconductor body, each memory cell comprising: a trench disposed within the semiconductor body (Fig 5; col 5, lines 20-52; Figs 1-4, 10d); a conductive material 34 filling at least a lower portion of the trench (Fig 5; col 5, lines 20-42); a dielectric material 32 lining sidewalls of the trench such that the conductive material filling the trench forms a first plate of a capacitor (col 4, lines 50-52; col 5, lines 20-52; Fig 5) and semiconductor material of the semiconductor body forms a second plate of the capacitor, the second plate of the capacitor being electrically coupled to capacitors of other memory cells within the array (Figs 5, 10b,1); a trench collar 30 lining a portion of a

sidewall of the trench above the dielectric material 32 (Fig 5; col 5, lines 26-42); a pass transistor having a first source/drain region and a second source/drain region 46, the first source/drain region 38 being electrically coupled to the conductive material 34 through an opening in the trench collar 30 (Fig 5), the opening formed at one side of the trench such that an asymmetric trench structure is formed (Fig 5); a plurality of wordlines extending along the rows of the array of memory cells, each wordline being electrically coupled to a gate of every other memory cell along the row (Figs 1,3,5; col 5, lines 1-20); a plurality of bitlines extending along the columns of the array of memory cells, each bitline being electrically coupled to the second source/drain region of every other memory cell along the column (Figs 1,3,5; col 5, lines 1-20); and a plurality of isolation regions 106 extending parallel to the plurality of bitlines and disposed between columns of the array of memory cells, each isolation region comprising a rectangular strip (Figs 3,1) of insulating material that extends between adjacent columns of the memory cells, wherein adjacent ones of the memory cells within a column are isolated without use of the isolation region (Figs 3,10d).

Re claim 62, wherein each isolation region (STI) has a width and is separated from a parallel isolation by a spacing distance, wherein the width is equal to the spacing distance (as shown in Fig 3). Re claim 63, wherein adjacent ones of the trenches are separated by a distance 3F, where F is a minimum feature size (as shown in Fig 3).
Re claim 64, wherein each pass transistor comprises a vertical transistor (col 5, lines 44-47).
Re claim 65, wherein, for each memory cell, the second source/drain region 46 is located at the surface of the semiconductor body and the first source/drain region 38 is located within the semiconductor body spaced from the surface (Fig 5; col 5, lines 43-52). Re claim 66, wherein the conductive material 34 filling at least the lower portion of the trench comprises doped polysilicon (col 5, lines 30-32). Re claim 67, wherein the second plate 22 of the capacitor comprises a doped region 22 of the semiconductor body that extends beneath ones of the trenches (Fig 5; col 5, lines 20-26).

Claim Rejections - 35 USC § 103

3. Claims 61-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arnold et al (2004/0238868) taken with Mandelman et al (6,339,241).

Arnold teaches memory cell device comprising: an array of memory cells arranged an array of rows and columns at the surface of a semiconductor body, each memory cell comprising: a trench disposed within the semiconductor body (Figs 1A,2,3,7,14C-21C); a conductive material filling at least a lower portion of the trench (Fig 2; paragraph 46); a dielectric material 29 lining sidewalls of the trench such that the conductive material filling the trench forms a first plate of a capacitor (paragraph 46; Fig 2)) and semiconductor material 26 of the semiconductor body forms a second plate of the capacitor, the second plate of the capacitor being electrically coupled to capacitors of other memory cells within the array (Figs 2,3,7); a trench collar 30 lining a portion of a sidewall of the trench above the dielectric material 29 (Fig 2; paragraph 46); a pass transistor having a first source/drain region 28 and a second source/drain region 38, the first source/drain region 28 being electrically coupled to the conductive material through an opening in the trench collar 30 (Fig 2; paragraph 47), the opening formed at both sides of the trench such that an symmetric trench structure is formed (Fig 2); a plurality of wordlines extending along the rows of the array of memory cells, each wordline being electrically coupled to a gate of every other memory cell along the row (Figs 1A-1B,2,3,7; paragraph 48); a plurality of bitlines extending along the columns of the array of memory cells, each bitline being electrically coupled to the second source/drain region of every other memory cell along the column (Figs 1A,1B,2,3,7, paragraph 48-50); and a plurality of isolation regions 10,68 extending parallel to the plurality of bitlines and disposed between columns of the array of memory cells, each isolation region comprising a rectangular strip (Fig 7; Fig 3, 6A-6B; paragraphs 60-63,75) of insulating material that extends between adjacent columns of the memory cells, wherein adjacent ones of the memory cells within a column are isolated without use of the isolation region (Figs 7;3,2,6A-6B). Re claim 62, wherein each isolation region (STI) has a width and is separated from a parallel isolation by a spacing distance, wherein the width is equal to the spacing distance (as shown in Fig 3). Re claim 63, wherein adjacent ones of the trenches are separated by a distance 3F, where F is a minimum feature size (as shown in Fig 2). Re claim 64, wherein each pass transistor comprises a vertical transistor (paragraphs 43,47). Re claim 65, wherein, for each memory cell, the second source/drain region 38 is located at the surface of the semiconductor body and the first source/drain region 28 is located within the semiconductor body spaced from the surface (Fig 2;

paragraph 47). Re claim 66, wherein the conductive material filling at least the lower portion of the trench comprises doped polysilicon (paragraph 46). Re claim 67, wherein the second plate of the capacitor comprises a doped region 26 of the semiconductor body that extends beneath ones of the trenches (Fig 2; paragraph 46).

Re claim 61, Arnold teaches forming openings in both trench collars (Fig 2); whereas, claim 61 recites forming an opening in one trench collar for an asymmetric trench structure.

However, Mandelman teaches a memory cell structure comprising an opening in one of the trench collars 30 for an asymmetric trench structure (Figs 5, col 5, lines 20-52; Figs 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory cell structure of Arnold by forming only an opening in one of the trench-collars, as taught by Mandelman. This is because of the desirability to form an asymmetric trench structure having single buried strap region on one side of the deep trench structure, thereby decreasing size of the memory structure and thus increasing array density.

Response to Amendment

4. Applicant's remarks and amendments filed September 20, 2006 with respect to new claims 61-67 have been considered but are moot in view of the new ground(s) of rejection.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oacs-18

Michael Trinh
Primary Examiner